Tutorial Title:
Circuit Board Layout for Wide Bandgap Power Transistors

Organizer:
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Abstract:
PCB layout is already challenging for power electronic circuits. But as wide-bandgap semiconductors (GaN and SiC) are increasingly adopted, their tenfold increase in switching speed compared to Silicon creates even more challenges for the circuit designer. Layout problems can lead to circuit malfunction, ringing and overshoot voltage spikes, EMI problems, higher loss than expected, and even transistor failure. Application notes often have the same advice to solve these problems: “be sure to minimize all parasitic layout inductance as much as possible.” But what is the best way to approach this, especially when there are multiple conflicting layout goals? It is simply not possible to eliminate all layout impedance everywhere, so how does one make the tradeoffs to optimize the PCB layout for best performance?

This seminar addresses these questions, and leads you through a process to understand where parasitic impedances really matter, understand the magnitude of parasitic impedances, evaluate layout options, and make an informed decision on how to proceed. The focus is on the primary-side power circuits, and is intended to cover the range from approximately 50 W to 5 kW.

Bio:
Eric Persson is a 40-year veteran of the power electronic industry. His career spans 19 years of hands-on power converter and inverter design, followed by 21 years in applications engineering in the semiconductor industry at Infineon Technologies (formerly International Rectifier). He is a Senior Principal Engineer for wide-bandgap semiconductor applications.

Eric has presented more than 90 tutorials and papers on topics related to applications and practical design aspects of power electronic circuits. He is a regular lecturer for power electronic short-courses at UW Madison for 20 years. Mr. Persson holds 15 patents, and is a recipient of the IEEE Third Millennium Medal. He has a BSEE degree from the University of Minnesota.